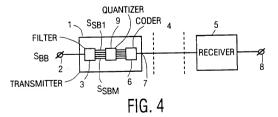


	FD1	FD2	:	FD3		
	SYNC AND SYSTEM INFO	ALLOCATION INFO	SCALE FACTORS	SAMPLES		DUMMY
IF			FIG 2		IP P'	IP P'+1

bo SYNC SIGNAL b15 b16, NMBR SLOTS b23 b24 FRÂME FORMAT INFO b31

FIG. 3



32-

BR bitrate (kbits/s)	Fs sample freq. (kHz)	B # slots in a frame
128	32 44.1 48	48 34 + padding 32
192	32 44.1 48	72 52 + padding 48
256	32 44.1 48	96 69 + padding 64
384	32 44.1	144 104 + padding

FIG. 5

bitrate (kbits/s)	total # frames in padding sequence	# frames with a dummy slot
128	147	122
192	49	12
256	147	97
384	49	24

F16.6

Bit 24 :	Frame type	0 format A 1 format B
Bits 25 and 26:		0 0 no copyright, own rec 0 1 no copyright, software 1 0 copyright, own record 1 1 copyright, software
Bits 27 - 31 :	Mode indication	
1 1 0 0 1 1 0 0 1 1 0 0 1 1 0 0 1 1 1 1	1 Stereo 0 Stereo 1 Stereo 0 Stereo 1 Stereo 1 Stereo 1 Stereo 1 Chan. 1 2 Chan. 0 2 Chan. 1 2 Chan. 1 2 Chan. 0 2 Chan. 1 1 Chan. 1 1 Chan. 0 1 Chan. 1 1 Chan.	48 kHz 50/15 µsec 144.1 kHz no emphasis 44.1 kHz no emphasis 32 kHz no emphasis 32 kHz no emphasis 50/15 µsec 150/15 µsec 150/
111	1 1 Chan	. 44.1 kHz CCITT J.17

F1G. 7

mode	channel	I	channel	II
stereo 2 channel mo 1 channel mo			right program not used	

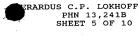
```
length of samples
allocation
info
                   in bits
                             (no samples or scale factors transferred)
0000
                   2
3
4
5
6
7
8
9
10
11
12
13
14
0001
0010
0011
0100
0101
0110
1000
1001
1010
1011
1100
1101
1110
                   not used to prevent incorrect sync detection
1111
```

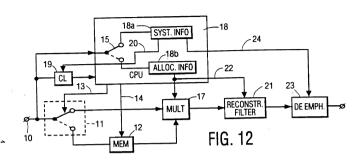
F16.9

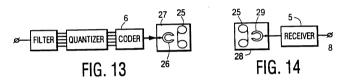
slot 2:						TT 4
I-1 II-1	I-2	II-2	I-3	II-3	I-4	II-4
slot 3:						
I-5 II-5	I - 6	II-6	エーフ	II-7	I-8	II-8
slot 4:						
I-9 II-9	I-10	II-10	/I-11	II-11	I-12	II-12
slot 5:						
I-13 II-13	I-14	II-14	I-15	II - 15	I-16	II-16
slot 6:				-		
I-17 II-17	I-18	II-18	I-19	II-19	I-20	II-20
slot 7:						
I-21 II-21	I-22	II-22	I-23	II-23	I-24	II-24
slot 8:						
I-25 II-25	I-26	II-26	I-27	II-27	I-28	II-28
slot 9:						
I-29 II-29	I-30	II-30	I-31	II-31	I-32	II-32

FIG. 10

	II-1	I-2	II-2	I-3	II-3	1-4	II-4
	11-5	I-6	II-6	I-7	II-7	I-8	II-8
_	II-9	1-10	11-10	I-11	II-11	I-12	II-12
slot I-13	5: II-13	I-14	II-14	I-15	II-15	I-16	II-16







SF I, m SF II, m	FD3 SAMPLES	IG. 15a
SF I, m	x SAMPLES I, m (y BITS/SAMPLE) x SAMPLES II, m (y BITS/SAMPLE)	FIG. 15b
SF I, m SF II, m	x SAMPLES m (z BITS/SAMPLE)	FIG. 15c
SF m	x SAMPLES I, m (y BITS/SAMPLE) x SAMPLES II. m (y BITS/SAMPLE)	FIG. 15d

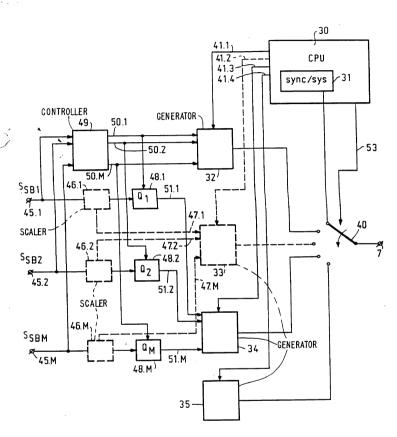


FIG.16

	BR	FU FRAME FORMAT
bo SYNC. SIGNAL	b15 616 HDEX b19 Fs	P b23 b24 INFO b31

FIG.17

Bits 16 to 19 : bitrate index

BR bitrate (kbits/ sec.)	BR index	sample frequenc 48 kHz # slots	Y I's 44.1 kHz # slots	32 kHz # slots
32 64 96 128 160 192 224 256 288 352 352 384 416	1 2 3 4 5 6 7 8 9 10 11 12 13	8 16 24 32 40 48 56 64 72 80 88 96 104	8 17 26 34 43 52 60 69 78 87 95 104 113 121	12 24 36 48 60 72 84 96 108 120 132 144 156

Bits 20 and 21 : Sample Frequency

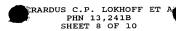
0 0 44.1 kHz 0 1 48 kHz 1 0 32 kHz 1 1 reserved

Bit 22 : padding bit

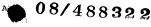
'l' if the frame contains a 'dummy' slot, Otherwise '0'

Bit 23 : Future Use

reserved for future use, '0' for the time being.







	DZ4 MODE	SWITCH	С	0/H	EMPH b31
--	----------	--------	---	-----	----------

FIG.19

Bits 24 and 25 : Mode indication

0 0 stereo 0 1 intensity stereo 1 0 bilingual

Bits 26 and 27 : Intensity stereo mode switches :

0 0 subbands 5-32 in intensity stereo mode 0 1 subbands 9-32 in intensity stereo mode 1 0 subbands 13-32 in intensity stereo mode 1 1 subbands 17-32 in intensity stereo mode

Bit 28 : Copyright 0 no copyright copyright protected

Bit 29 : Original/Home Copy 0 Copy 1 Original

Rite 30 and 31 : Emphasis 0 0 no emphasis

Bits 30 and 31 : Emphasis 0 0 no emphasis 0 1 50/15 μ sec emphasis 1 0 reserved

1 1 CCITT J.17

FIG. 20

Mono mode :

M = mono signal

slot 2: M-8 M-7M-2 M-3M-4 M-5 M-6 M-1slot 3: M-16 M-15 M-13 M-14 M-10 M-11 M-12 slot 4: M = 24M-23 M-17 M-18 M-19 M-22 slot 5: M - 32M-29 M - 30M-31 M-26 M-27 M-28



Intensity Stereo mode :

```
L = left channel, R = right channel, M = mono signal
Switch bits (bits 26 and 27) are 0 0:
slot 2:
                                        L-4 R-4
                       R-2
                             L-3 R-3
           R-1
                L-2
     L-1
slot 3:
     M-5
           M-6
                 M-7
                       M-8
                             M-9
                                   M-10 M-11 M-12
slot 4:
     M-13
           M-14 M-15
                       M-16
                            M-17 M-18
                       M-24 M-25
                                 M-26 M-27
                                             M-28
     M-21
           M-22
                M-23
slot 6:
                       M-32
     M-29
           M-30 M-31
                                              FIG. 22a
Switch bits are 0 1 :
slot 2:
                                   R-3 L-4
                                               12-4
                 L-2
                        R-2
                            L-3
           R-1
      L-1
slot 3:
                                   R-7
                                         L-8
                                               R-8
                 L-6
                       R-6
                            L-7
           R-5
slot 4:
                                   M-14 M-15
                       M-12 M-13
                                               M - 16
      M-9
           M-10 M-11
slot 5:
                                   M-22
                                               M-24
                       M-20
                             M-21
                 M-19
           M-18
 slot 6:
                                   M-30
                                        M-31
                             M-29
                                              M-32
                        M-28
           M-26
      M-25
                                              FIG. 22b
Switch bits are 1 0 :
slot 2:
                                               R = h
                                        L-4
                             L-3
                                   R-3
                  L-2
                        R-2
           R-1
slot 3:
                                        L-8
                             L-7
                                   R-7
                                               R-8
                 L-6
                        R-6
           R-5
slot 4:
                                        L-12 R-12
                  L-10 R-10 L-11 R-11
      L-9
           R-9
slot 5:
                        M-16 M-17
                                   M-18
                                         M-19
                                               M - 20
      M-13
           M-14 M-15
slot 6:
                                         M-27
                                               M-28
                       M-24
     M-21
           M-22
                M-23
slot 7:
                       M - 32
     M-29 :M-30 M-31
                                              FIG. 22c
Switch bits are 1 1:
slot 2:
                           L-3 R-3 L-4 R-4
                 L-2
     L-1
           R-1
                       R-2
slot 3:
                                   R-7 L-8
                                             R-8
     L-5
           R-5
                 L-6
                       R-6
slot 4:
                       R-10 L-11 R-11
     T.-9
           R-9
                 L-10
slot 5:
                                        L-16
                                             R-16
                       R-14 L-15 R-15
     L-13
           R-13
                 L-14
slot 6:
                       M-20 M-21 M-22 M-23
                                              M - 24
     M-17
          M-18
                M-19
                                              m-32 FIG.22d
slot 7:
                            M-29 M-30 M-31
     M-25 M-26 M-27
                       M-28
```

